# LM64C15P
## Passive Matrix Color LCD Unit

### FEATURES

- Display Format: 640 (W) × 480 (H)
- Overall Dimensions:
  243.5 (W) × 179.9 (H) × 10 max (D) mm
- Active Area: 195 (W) × 147 (H) mm
- Backlight: CCFT
- Dot Pitch:
  0.07 × RGB (W) × 0.275 (H) mm

### DESCRIPTION

The SHARP LM64C15P is a 640 × 480 dot color display unit consisting of an LCD panel, Printed Wiring Board (PWB) with electric components mounted on it, Tape Automated Bonding (TAB) to connect the LCD panel and PWB electrically, and a plastic chassis with a CCFT backlight and bezel to fit them mechanically. Signal ground ($V_{SS}$) is connected with the metal bezel. A DC/DC converter is built in.

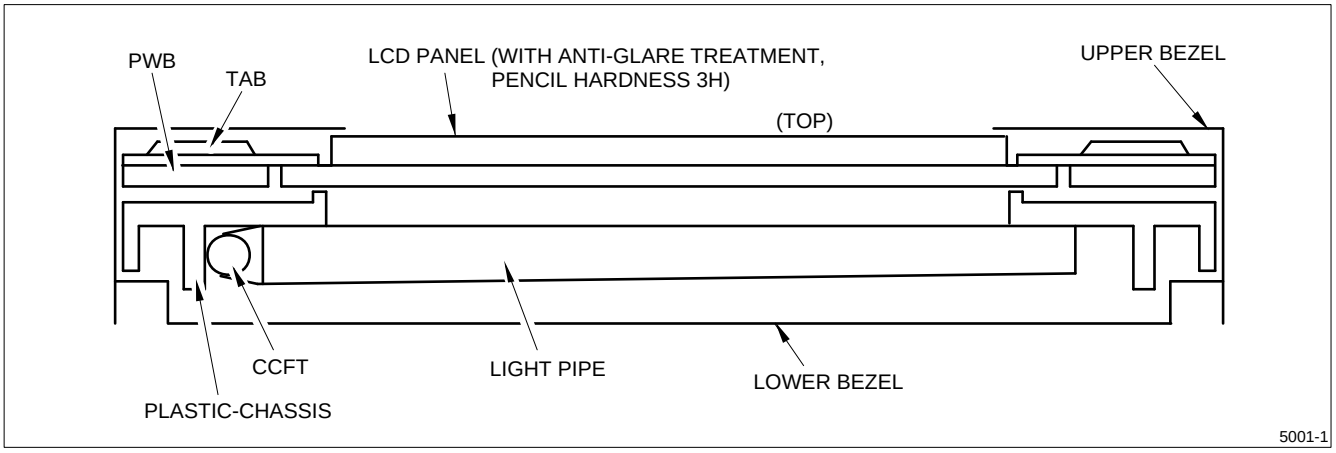



**Figure 1. LM64C15P Construction**

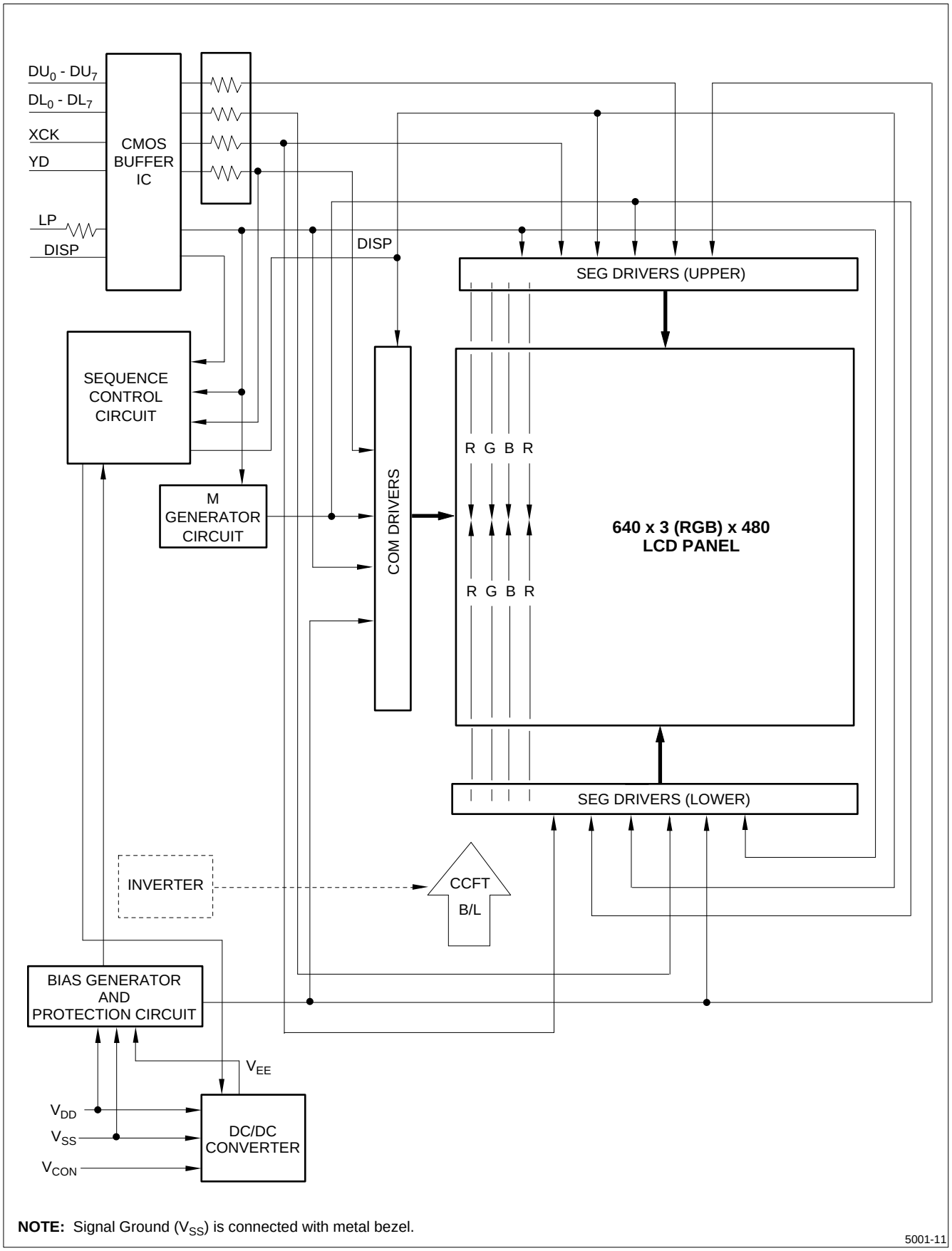



**Figure 2. LM64C15P Block Diagram**

## MECHANICAL SPECIFICATIONS

| PARAMETER | SPECIFICATIONS | UNIT | NOTE |
|---|---|---|---|
| Outline Dimensions | 243.5 (W) × 179.9 (H) × 10 max (D) | mm | – |
| Active Area | 195 (W) × 147 (H) | mm | – |
| Display Format | 640 (W) × 480 (H) Full Dots | – | – |
| Dot Size | 0.075 × RGB (W) × 0.275 (H) | mm | – |
| Dot Spacing | 0.025 | mm | – |
| Base Color | Normally Black | – | 1, 2 |
| Weight | Approximately 490 | g | – |

**NOTES:**

1. Due to the characteristics of the LC material, the colors vary with environmental temperature.
2. Negative-type display:
   Display data 'H': ON: → Transmission
   Display data 'L': OFF: → Light isolation

## ABSOLUTE MAXIMUM RATINGS ($t_A$ = 25°C)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $V_{DD} - V_{SS}$ | Supply Voltage (Logic) | 0 | 6.0 | V |
| $V_{IN}$ | Input Voltage | −0.3 | $V_{DD}$ + 0.3 | V |

## ENVIRONMENTAL CONDITIONS

| ITEM | Tstg | | Topr | | CONDITION | NOTE |
|---|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | | |
| Ambient Temperature | −25°C | +60°C | 0°C | +40°C | | 1 |
| Humidity | – | | | | No condensation | 2 |
| Vibration | – | | | | 3 Directions (X/Y/Z) | 3 |
| Shock | – | | | | 6 Directions (±X ±Y ±Z) | 4 |

**NOTES:**

1. Do not subject the LCD unit to temperatures out of this specification.
2. $t_A \leq 40°C$, 95% RH maximum.
   $t_A > 40°C$, Absolute humidity shall be less than $t_A = 40°C$ at 95% RH.
3. These test conditions are in accordance with 'IEC 68-2-6' as shown in the following table (two hours for each direction of X/Y/Z (six hours total)):

| | | |
|---|---|---|
| Frequency | 10 Hz to 57 Hz | 57 Hz to 500 Hz |
| Vibration Level | – | 9.8 $m/s^2$ |
| Vibration Width | 0.075 mm | – |
| Interval | 10 Hz to 500 Hz to 10 Hz/11 min | |

4. Acceleration: 490 $m/s^2$
   Pulse width: 11 ms
   Three times for each direction of ±X/±Y/±Z.

## ELECTRICAL CHARACTERISTICS ($t_A$ = 25°C, $V_{DD}$ = 5 V ±10%)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT | CONDITION | NOTE |
|---|---|---|---|---|---|---|---|
| $V_{DD} – V_{SS}$ | Supply Voltage (Logic) | 4.5 | 5.0 | 5.5 | V | – | 1 |
| $V_{CON} – V_{SS}$ | Contrast Adjust Voltage | 0.8 | – | – | V | $t_A$ = 0°C | – |
| | | 1.35 | 1.95 | 2.55 | V | $t_A$ = 25°C | – |
| | | – | – | 2.80 | – | $t_A$ = 40°C | – |
| $V_{IN}$ | Input Signal Voltage | 0.8 $V_{DD}$ | $V_{DD}$ | VDD + 0.3 | V | 'H' Level | – |
| | | –0.3 | $V_{SS}$ | 0.2 VDD | V | 'L' Level | – |
| $I_{IL}$ | Input Leakage Current | – | – | 1.0 | µA | 'H' Level | – |
| | | –1.0 | – | – | µA | 'L' Level | – |
| $I_{DD}$ | Supply Current (Logic) | – | 160 | 240 | mA | – | 2 |
| $I_{RUSH}$ | Rush Current (Logic) | 3 A (pk) × 25 ms + 1 A (pk) × 10 µs max | | | | $t_A$ = 25°C Power ON | – |
| $P_D$ | Power Consumption | – | 800 | 1320 | mW | – | 2 |

**NOTE:**

1. Under the following conditions:
   a. Immediately after the rise of DISP signal: 3A × 25 ms
   b. When DISP signal is on and kept steady: 1 A × 10 µs
2. Under the following conditions:
   $V_{CON} – V_{SS}$: contrast maximum (1.95 V, TYP)
   $V_{DD} – V_{SS}$ = 5 V, frame frequency = 73 Hz, display pattern = black/white stripe pattern.
   This value is direct current. (Refer to Figure 3.)

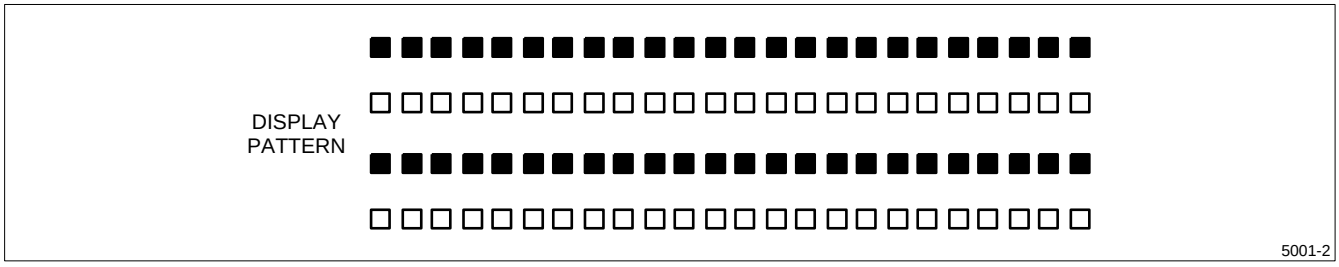



**Figure 3. Display High Frequency Pattern**

## INTERFACE SIGNALS

### LCD [1]

| PIN NUMBER [2] | SYMBOL | PARAMETER | LEVEL |
|---|---|---|---|
| 1 | $DL_4$ | Display Data Signal (Lower) | H (ON), L (OFF) |
| 2 | $V_{SS}$ | Ground Potential | – |
| 3 | $DL_5$ | Display Data Signal (Lower) | H (ON), L (OFF) |
| 4 | YD | Scan Start-Up Signal | 'H' |
| 5 | $DL_6$ | Display Data Signal (Lower) | H (ON), L (OFF) |
| 6 | LP | Input Data Latch Signal | 'H' → 'L' |
| 7 | $DL_7$ | Display Data Signal (Lower) | H (ON), L (OFF) |
| 8 | $V_{SS}$ | Ground Potential | – |
| 9 | $V_{SS}$ | Ground Potential | – |
| 10 | XCK | Data Input Clock Signal | 'H' → 'L' |
| 11 | $DL_0$ | Display Data Signal (Lower) | H (ON), L (OFF) |
| 12 | $V_{CON}$ | Contrast Adjust Voltage | – |
| 13 | $DL_1$ | Display Data Signal (Lower) | H (ON), L (OFF) |
| 14 | $V_{DD}$ | Power Supply for Logic and LCD (+5 V) | – |
| 15 | $V_{SS}$ | Ground Potential | – |
| 16 | $V_{DD}$ | Power Supply for Logic and LCD (+5 V) | – |
| 17 | $DL_2$ | Display Data Signal (Lower) | H (ON), L (OFF) |
| 18 | DISP | Display Control Signal | H (ON), L (OFF) |
| 19 | $DL_3$ | Display Data Signal (Lower) | H (ON), L (OFF) |
| 20 | NC | – | – |
| 21 | $V_{SS}$ | Ground Potential | – |
| 22 | $DU_3$ | Display Data Signal (Upper) | H (ON), L (OFF) |
| 23 | $DU_4$ | Display Data Signal (Upper) | H (ON), L (OFF) |
| 24 | $DU_2$ | Display Data Signal (Upper) | H (ON), L (OFF) |
| 25 | $DU_5$ | Display Data Signal (Upper) | H (ON), L (OFF) |
| 26 | $DU_1$ | Display Data Signal (Upper) | H (ON), L (OFF) |
| 27 | $V_{SS}$ | Ground Potential | – |
| 28 | $DU_0$ | Display Data Signal (Upper) | H (ON), L (OFF) |
| 29 | $DU_6$ | Display Data Signal (Upper) | H (ON), L (OFF) |
| 30 | $V_{SS}$ | Ground Potential | – |
| 31 | $DU_7$ | Display Data Signal (Upper) | H (ON), L (OFF) |

**NOTES:**

1. Connector used: DF9B-31P-1V (HIROSE)
   Mating connector: DF9B-31S-1V (HIROSE)
2. Pin number and its locations are shown in the Outline Dimensions diagram.

## CCFT [1]

| PIN NUMBER [2] | SYMBOL | DESCRIPTION | LEVEL |
|---|---|---|---|
| 1 | HV | High Voltage Lineal (From Inverter) | – |
| 2 | NC | – | – |
| 3 | GND | Ground Line (From Inverter) | – |

**NOTES:**

1. Connector used: BHR-03VS-1 (JST)
   Mating connector: SM03 (4.0) B-BHS or SM02 (8.0) B-BHS (JST)
2. Pin number and its locations are shown in the Outline Dimensions diagram.

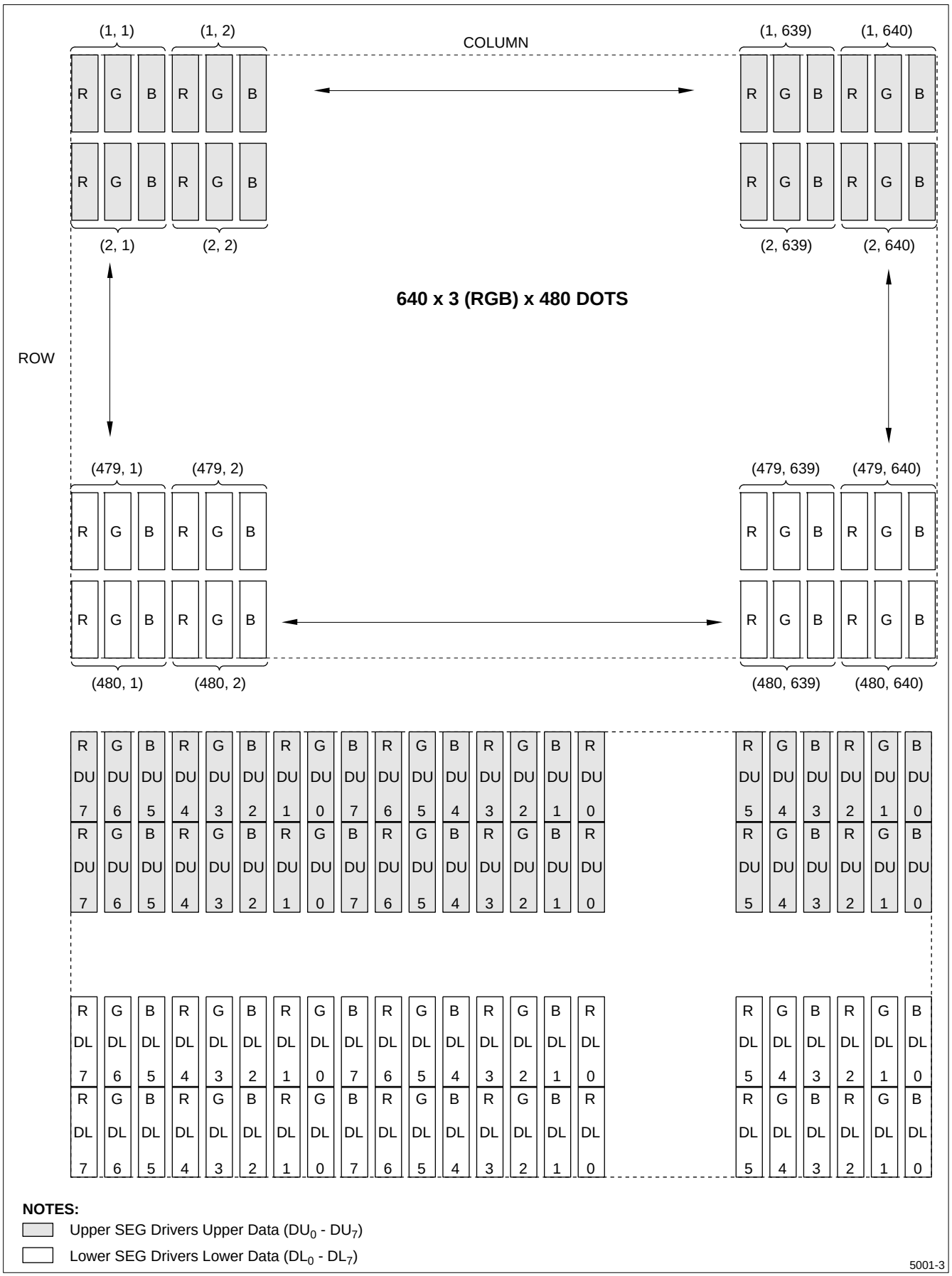



**Figure 4. Dot Chart of Display Area**

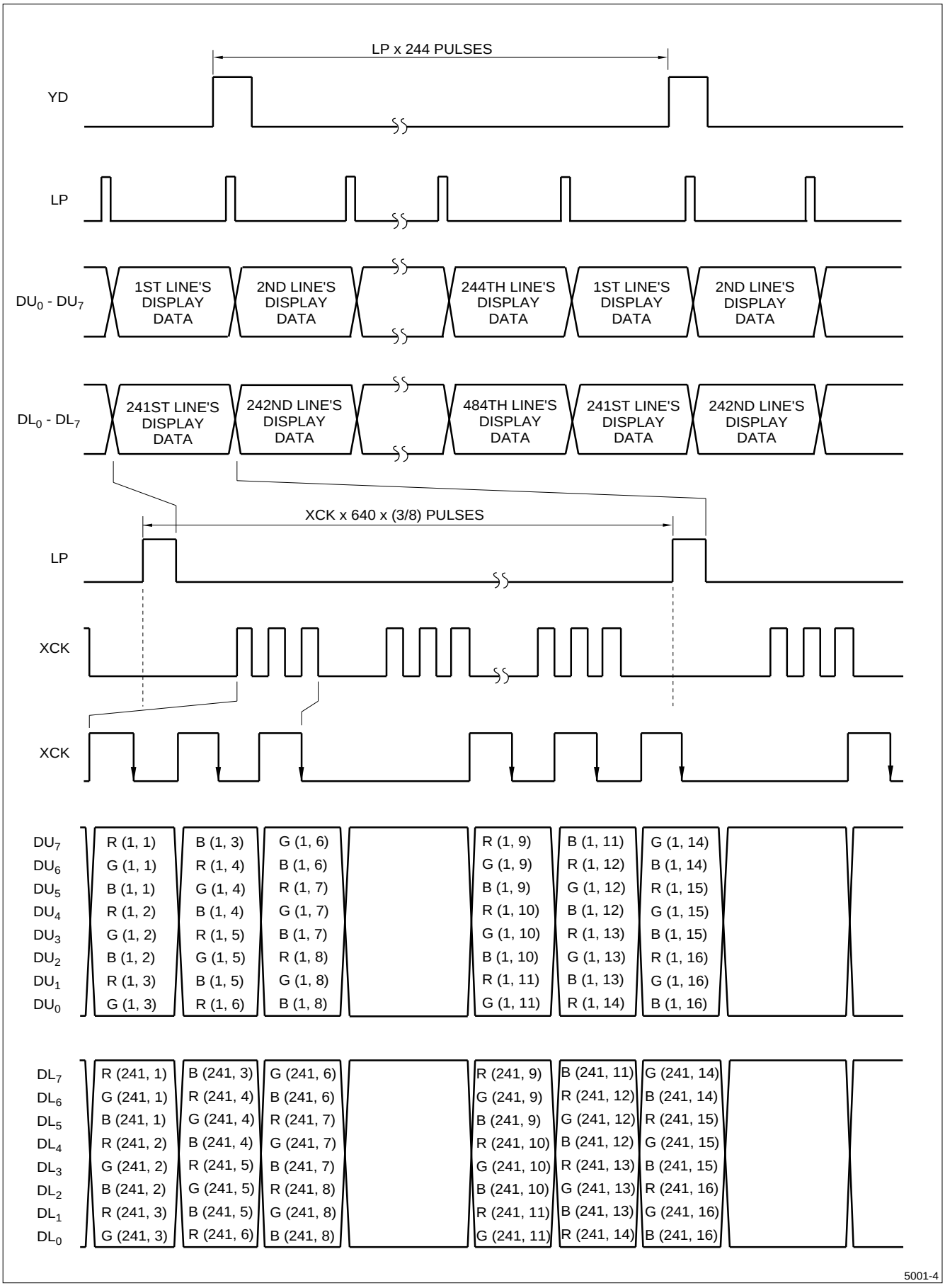



**Figure 5. Data Input Timing**

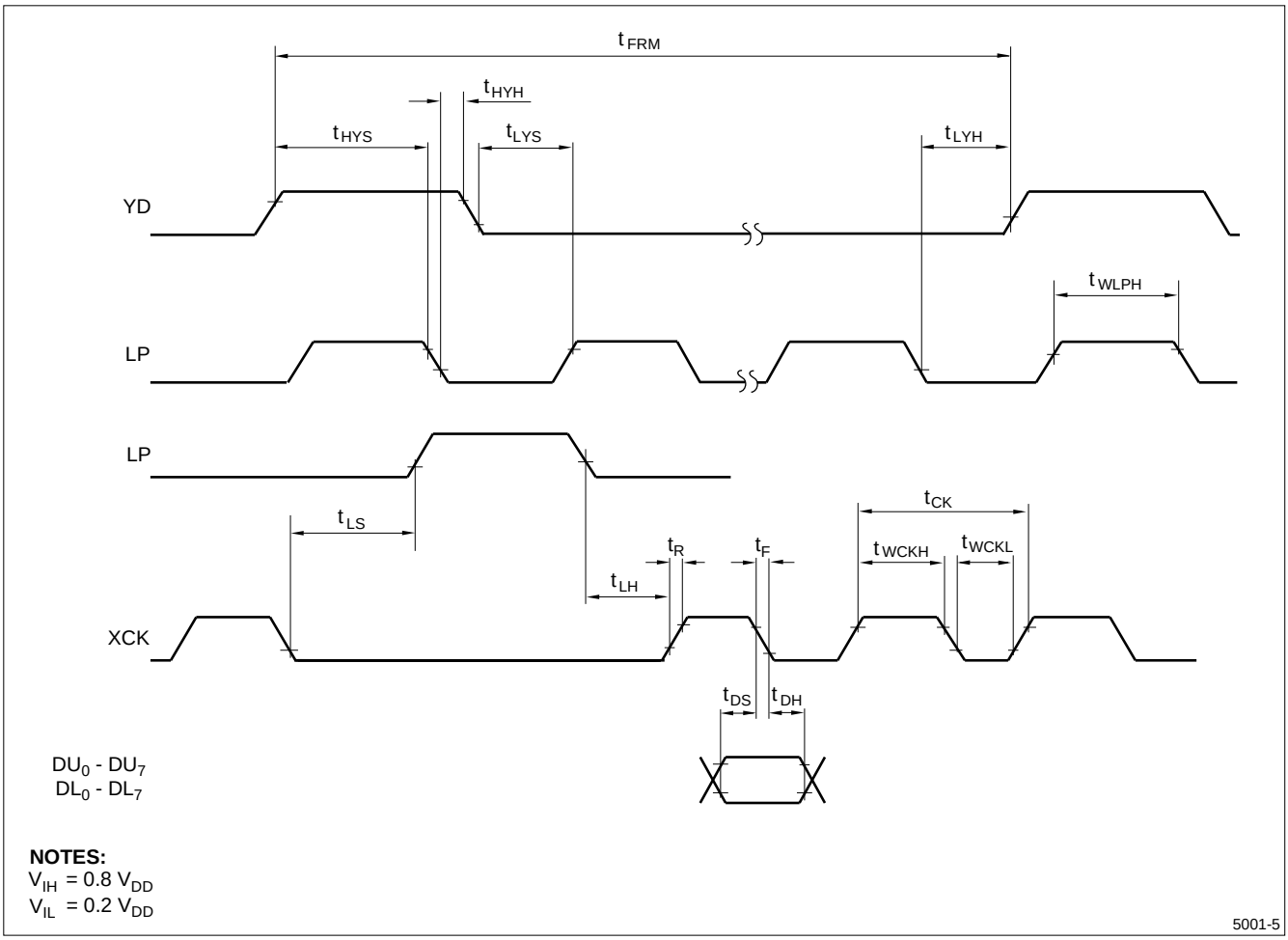



**Figure 6. Interface Timing Chart**

## INTERFACE TIMING RATINGS

| SYMBOL | PARAMETER | | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| $t_{FRM}$ | Frame Cycle | | 8.33 | – | 16.94 | ms | 1 |
| $t_{HYS}$ | YD Signal | 'H' Level Setup Time | 100 | – | – | ns | – |
| $t_{HYH}$ | | 'H' Level Hold Time | 100 | – | – | ns | – |
| $t_{LYS}$ | | 'L' Level Setup Time | 100 | – | – | ns | – |
| $t_{LYH}$ | | 'L' Level Hold Time | 40 | – | – | ns | – |
| $t_{WLPH}$ | LP Signal 'H' Level Pulse Width | | 200 | – | – | ns | – |
| $t_{CK}$ | XCK Signal | Clock Cycle | 82 | – | – | ns | – |
| $t_{WCKH}$ | | 'H' Level Clock Width | 30 | – | – | ns | – |
| $t_{WCKL}$ | | 'L' Level Clock Width | 30 | – | – | ns | – |
| $t_{DS}$ | Data Setup Time | | 30 | – | – | ns | – |
| $t_{DH}$ | Data Hold Time | | 30 | – | – | ns | – |
| $t_{LS}$ | LP ↑ Allowance Time From XCK ↓ | | 200 | – | – | ns | – |
| $t_{LH}$ | XCK ↑ Allowance Time From LP ↓ | | 200 | – | – | ns | – |
| $t_R$, $t_F$ | Input Signal Rise/Fall Time | | – | – | 13 | ns | – |

**NOTE:**

1. The LCD unit functions at the minimum frame cycle of 8.33 ms (maximum frame frequency of 120 Hz). Due to the characteristics of the LCD unit, 'shadowing' becomes more evident as frame frequency goes up, while flicker is reduced.

   According to our experiments, a minimum frame cycle of 12.8 ms or a maximum frame frequency of 78 Hz demonstrates optimum display quality in terms of flicker and 'shadowing.' Since visual judgment of display quality is subjective, and display quality such as 'shadowing' is pattern dependent, base frame frequency cycle, to which power consumption of the LCD unit is proportional, on thorough testing of the LCD unit with every possible pattern displayed on it.

## UNIT DRIVING METHOD

### Circuit Driving Method

Figure 2 shows the block diagram of the unit's circuitry.

### Display Face Configuration

The display consists of 640 × 3 (RGB) × 480 dots as shown in Figure 4. The is a single panel with double drive driven at 1/244 duty interface ratio.

### Input Data and Control Signal

The LCD driver is 160 bits LSI, consisting of shift registers, latch circuits, and LCD driver circuits. Input data for each row (640 × 3 RGB) is sequentially transferred in the form of 8-bit parallel data through shift registers from the top left of the display together with the Clock Signal (XCK).

When input of one row (640 × 3 RGB dots) is completed, the data is latched in the form of parallel data corresponding to the signal electrodes by the falling edge of the Latch Signal (LP). Then the corresponding drive signals are transmitted to the 640 × 3 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, the scan start-up signal (YD) is transferred from the scan signal driver to the first row of scan electrodes, and the contents of the data signals are displayed on the first row of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the first row of data for dots is being displayed, the second row of data is entered. When 640 × 3 dots of data have been transferred, they are latched by the falling edge of LP, switching the display to the second row.

Such data input is repeated up to the 244th row of each display segment, from upper to lower rows, to complete one frame of display using the time-sharing method.

Simultaneously, the same scanning sequence occurs at the lower panel. Then data input proceeds to the next display frame.

YD generates the scan signal to drive horizontal electrodes.

Since DC voltage, if applied to the LCD panel, causes chemical reaction which deteriorates the LCD panel, drive waveforms are inverted at every display frame by Control Signal M to prevent the generation of such DC voltage.

Because of the characteristics of the CMOS driver LSI, the power consumption of the unit goes up with the clock frequency XCK. To minimize data transfer speed of XCK clock, the LSI transfers 8 bits of parallel data through the eight lines of shift registers. This system minimizes power consumption of the display unit.

In this circuit configuration, 8-bit display data are input to data pins $DU_0$ – $DU_7$ and $DL_0$ – $DL_7$.

The LCD unit also has a bus line system for data input to minimize the power consumption. In this system, the data input terminal of each driver LSI is activated only when relevant data input is fed.

Data input for column electrodes and the chip select of driver LSI are made as follows:

- The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when data of 160 dots (20 XCK) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face.
- This process is immediately followed both at the top and bottom column driver's LSIs. Thus, data input will be made through 8-bit bus line sequentially from the left end of the display face.

Since this display unit contains no refresh RAM, it requires the above data and timing pulse inputs even for static display.

The timing chart of input signals is shown in Figure 6 and the Interface Timing Ratings table.

## OPTICAL CHARACTERISTICS ($t_A$ = 25°C, $V_{DD}$ = 5.0 V, $V_{CON}$ – $V_{SS}$ = Vmax)

The following specifications are based on the electrical measuring conditions, on which the contrast of perpendicular direction (θx = θy = 0°) is maximum.

| SYMBOL | PARAMETER | CONDITION | | MIN | TYP | MAX | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|
| θx | Viewing Angle Range | $C_0$ > 5.0 | θy = 0° | –30 | – | 30 | degrees | 1 |
| θy | | | θx = 0° | –25 | – | 15 | | |
| $C_0$ | Contrast Ratio | θx = θy = 0° | | 10 | 18 | – | – | 2 |
| $t_R$ | Response Time – Rise | θx = θy = 0° | | – | 210 | 290 | ms | 3 |
| $t_D$ | Response Time – Decay | θx = θy = 0° | | – | 90 | 110 | ms | |
| x | Unit Chromaticity – White | θx = θy = 0° | | – | 0.277 | – | – | – |
| y | | θx = θy = 0° | | – | 0.329 | – | – | – |

**NOTES:**

1. The viewing angle is shown in Figure 7.
2. Contrast Ratio is defined as follows:

$$Co = \frac{\text{Luminance (brightness) all pixels 'white' at } V_{MAX}}{\text{Luminance (brightness) all pixels 'dark' at } V_{MAX}}$$

   $V_{MAX}$ is defined in Figure 9.
3. The Response characteristics of the photodetector output are measured as shown in Figure 10, assuming that input signals are applied to select and deselect the dots to be measured, in the optical characteristics test method shown in Figure 11.

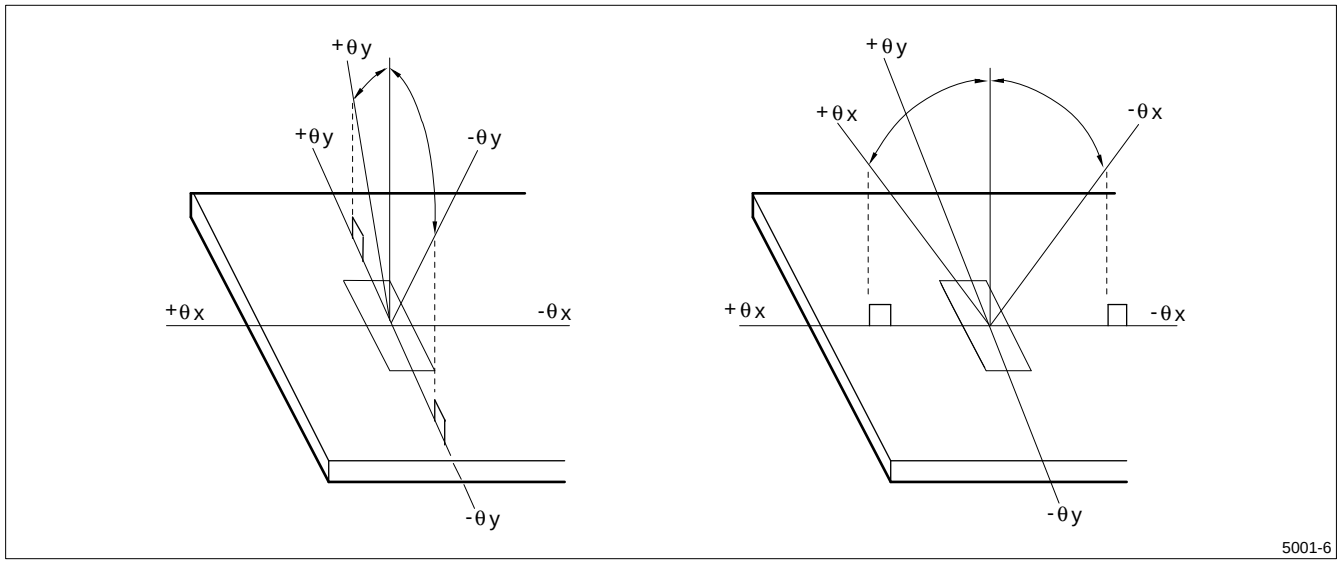



**Figure 7. Definition of Viewing Angle**

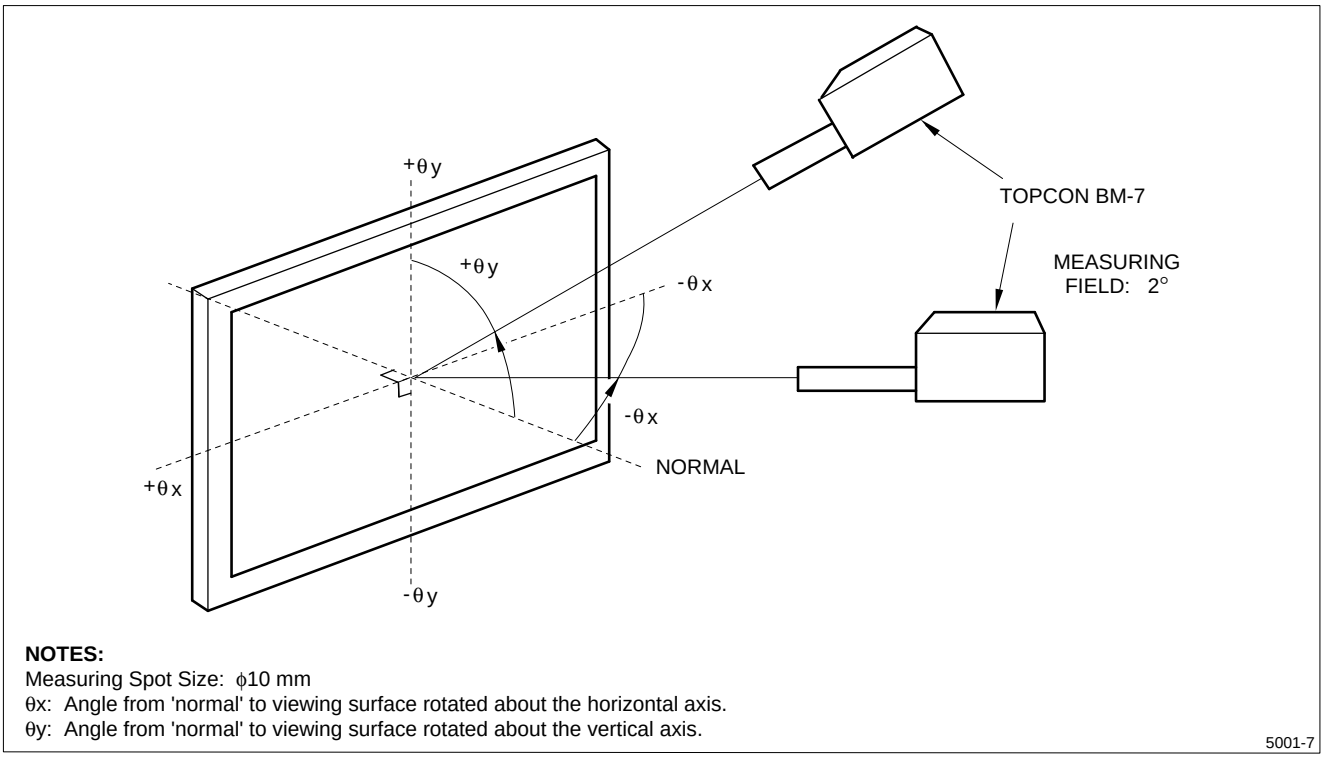



**Figure 8. Optical Characteristics Test Method I**

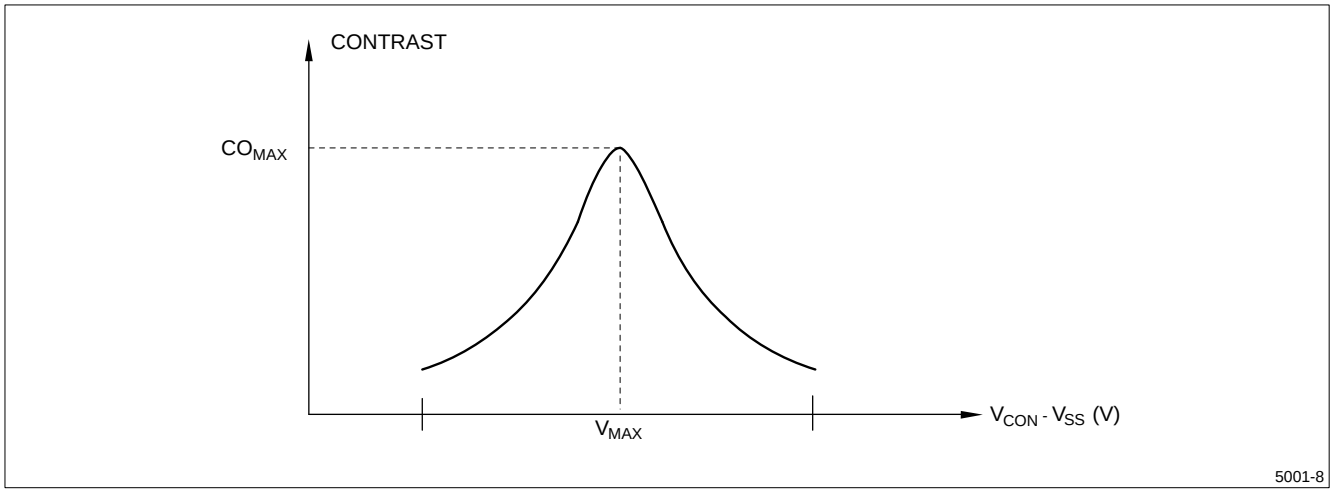



**Figure 9. Definition of $V_{MAX}$**

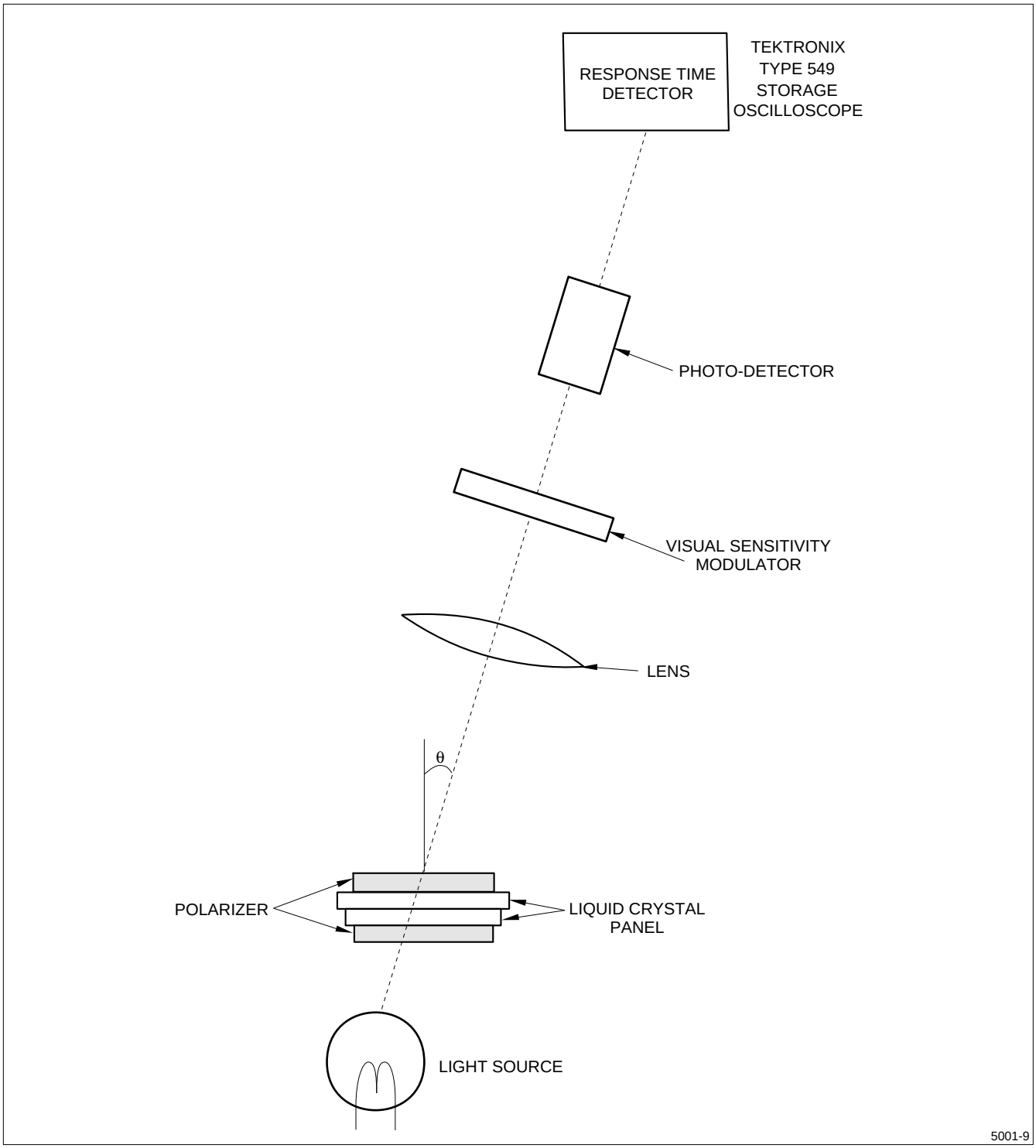



**Figure 10. Optical Characteristics Test Method II**

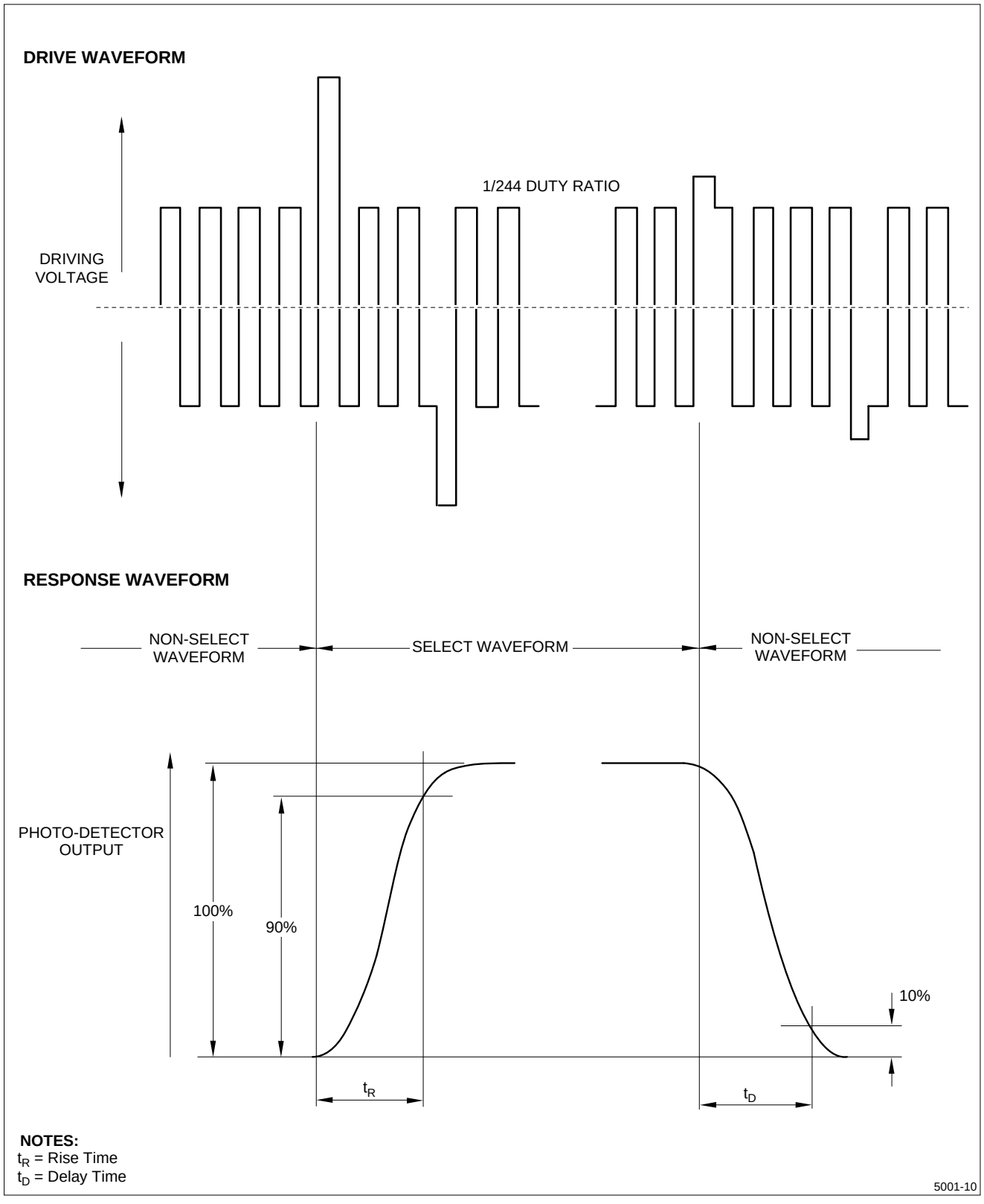



**Figure 11. Definition of Response Time**

## CHARACTERISTICS OF BACKLIGHT

The ratings satisfy the following conditions.

### Rating

| PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|
| Brightness | 60 | 80 | – | $cd/m^2$ |

### Measurement Circuit

CXA-M10L (TDK) (at IL = 6 mA RMS)

### Measurement Equipment

BM-7 (TOPCON Corporation)

### Measurement Conditions

- Measurement circuit voltage: DC = 10.6 V at primary side.
- LCD: All digits WHITE, $V_{DD}$ = 5 V, $V_{CON} – V_{SS} = V_{MAX}$, $DU_0 – DU_7$ = 'H' (WHITE), $DL_0 – DL_7$ = 'H' (WHITE).
- Ambient temperature: 25°C. Make measurement 30 minutes after turning on the unit.

### Lamp Used (Ratings, 1pc.)[1]

K-C211T30E50BH Western Electric, LTD., 1 pc.

| PARAMETER | | MAXIMUM ALLOWABLE VALUE | NOTE |
|---|---|---|---|
| Circuit Voltage (VS) | 1,300 $V_{RMS}$ (minimum) | – | 4 |
| Discharging Tube Current (IL) | 6 $mA_{RMS}$ (typical) | 6.5 $mA_{RMS}$ | 2 |
| Power Consumption (P) | 2.6 W | – | 3 |
| Discharging Tube Voltage (VL) | 430 ±43 $V_{RMS}$ | – | – |
| Brightness (B) | 30,000 $cd/m^2$ (typical) | – | – |

**NOTES:**

1. Within no conductor closed (CCFT only).
2. It is recommended that IL is not more than 6 $mA_{RMS}$ so that heat radiation of the CCFT backlight least affects the display quality.
3. Power consumption excludes inverter loss.
4. The circuit voltage (VS) of the inverter should be designed to have some margin (reference value: 1,450 $V_{RMS}$ minimum), because VS may be increased due to the leak current in the LCD unit.

### Operating Life

The operating lifetime is 10,000 hours or more at 6 mA (5,000 hours or more at 6.5 mA) (operating life with CXA-M10L or equivalent).

The inverter should meet the following conditions to keep the specific lifetime of the lamp used:

- Sine, symmetric waveform without spike in positive and negative.
- Output frequency range is from 25 kHz to 45 kHz.

Allow sufficient burn-in time before executing the operating conditions.

The operating lifetime is defined as having ended when any of the following conditions occur (25 ±1°C):

- When the voltage required for initial discharge has reached 1430 $V_{RMS}$, or when it has reached 12.0 VDC when an inverter is used.
- When the illuminence or quantity of light has decreased to 60% of the initial value.

***NOTE:*** Ratings are defined as the average brightness inside the viewing area specified in Figure 12.

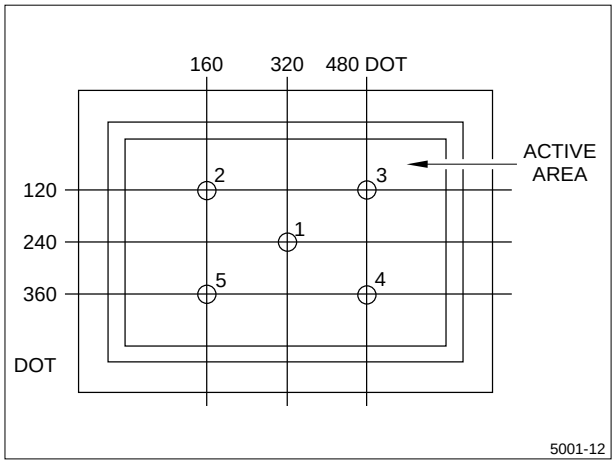



**Figure 12. Measuring Points (1 to 5)**

## PRECAUTIONS

- Industrial (Mechanical) design of the product in which this LCD unit is incorporated must be made so that the viewing angle characteristics of the LCD are optimized. This unit's viewing angle is illustrated in Figure 13 and is as follows:
  - θy MIN < viewing angle < θy MAX
    (For the specific values of θy MIN, θy MAX, refer to the Optical Characteristics table.) Consider the optimum viewing conditions according to their purpose when installing the unit.

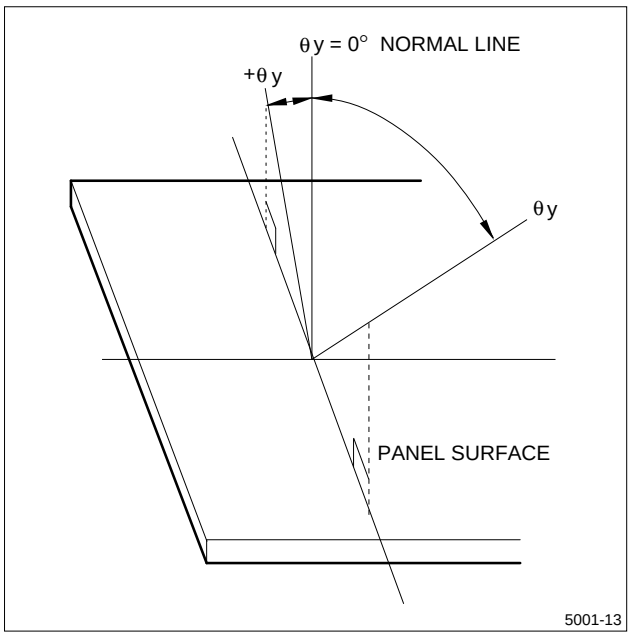



**Figure 13. Dot Matrix LCD Viewing Angle**

- This unit is installed using mounting tabs at the four corners of the PCB or bezel. During installation, avoid undue stress on the unit such as twisting or bending. A transparent acrylic resin board or other type of protective panel should be attached to the front of the unit to protect the polarizer, LCD cells, etc.
- Since the front polarizer is easily damaged, use care to not scratch the face.
- If the surface of the LCD cells need cleaning, wipe it with a soft cloth.
- Wipe liquid off immediately since it can cause color changes and staining.
- The LCD is made of glass plates, use care when handling it to avoid breakage.
- This unit contains CMOS LSIs which are sensitive to electrostatic charges. The following measures should be taken to protect the unit from electrostatic discharge:
  - Ground the metallic case of the main system (contact of the unit and main system).
  - Insulate the unit and main system by attaching insulating washers made of bakelite or nylon.
- The unit should be driven according to the specified ratings to avoid the malfunction of permanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is an alternating waveform by continuously applying signal M. Avoid latch-up of driver LSIs and application of DC voltage to the LCD panel by following the ON/OFF sequency shown in Figure 14 and Table 1.
- Since leakage current may affect brightness of the display (which may be caused by the routing of CCFT cables, etc.), design the inverter by taking the leakage current into consideration. Thoroughly evaluate the LCD unit/inverter built into its host equipment to ensure the specified brightness.
- Do not expose the unit to direct sunlight, strong ultraviolet light, etc., for prolonged periods.
- Store the unit at normal room temperature to prevent the LC from converting to liquid (due to excessive temperature changes).
- Do not disassemble the unit.

## SUPPLY VOLTAGE SEQUENCE CONDITION

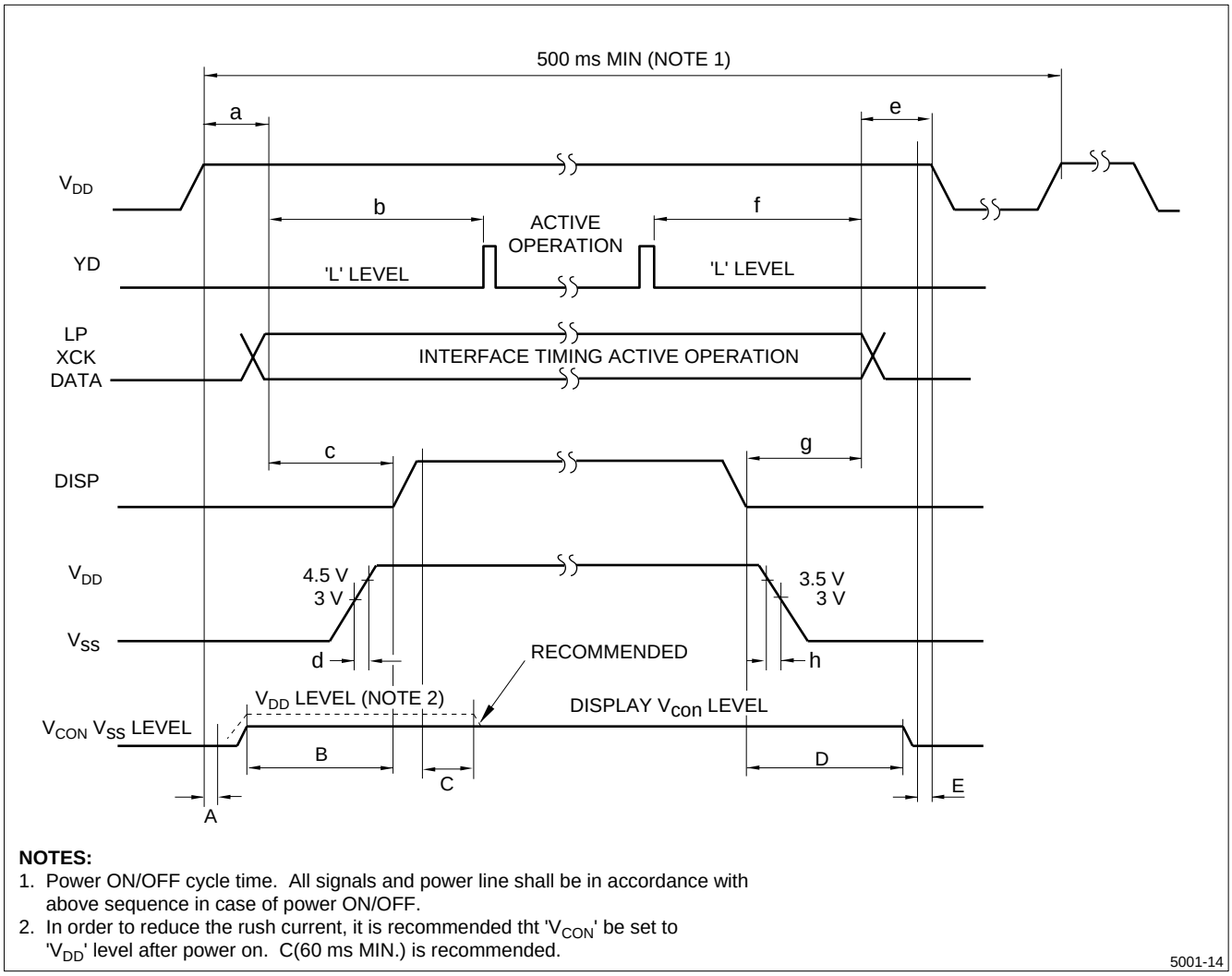
Refer to Figure 14 and Table 1.

**Table 1. Supply Voltage Sequence Condition**

| SYMBOL | CONDITION |
|---|---|
| **POWER ON** | |
| a | 0 ms (minimum) |
| b | 0 ms (minimum) |
| c | LP × 250 (minimum) |
| d | 25 ms (maximum) |
| A | 0 ms (minimum) |
| B | 0 ms (minimum) |
| C | 60 ms (minimum) [1] |
| **POWER OFF** | |
| e | 0 ms (minimum) |
| f | 0 ms (minimum) |
| g | 0 ms (minimum) |
| h | 1 ms (minimum) |
| D | 0 ms (minimum) |
| E | 0 ms (minimum) |

**NOTE:**

1. Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.




**NOTES:**
1. Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.
2. In order to reduce the rush current, it is recommended tht '$V_{CON}$' be set to '$V_{DD}$' level after power on. C(60 ms MIN.) is recommended.

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**Figure 14. Supply Voltage Sequence Condition**

## APPLICABLE INSPECTION STANDARD

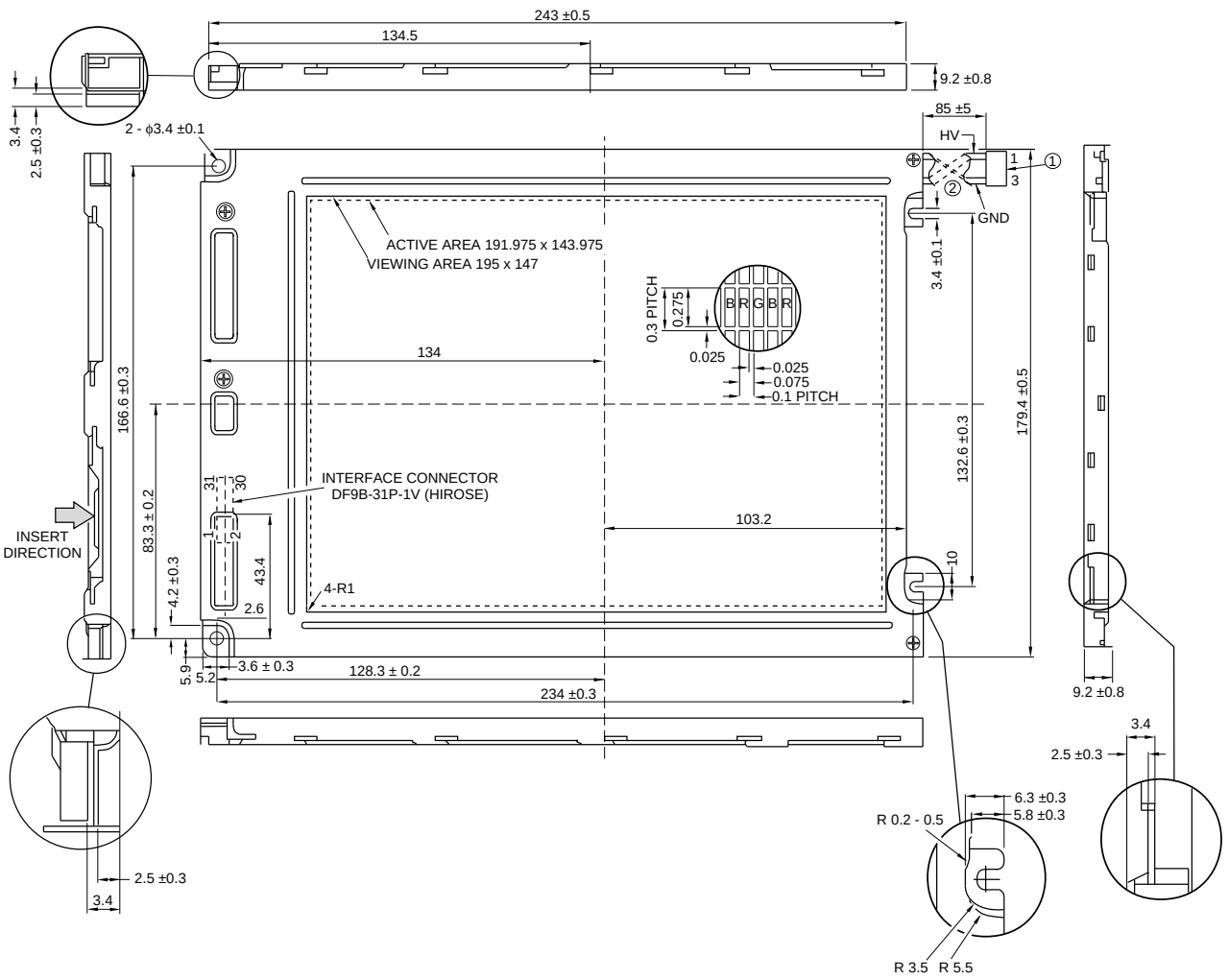
The LCD unit meets the following inspection standard: S-U-014

## DISPLAY QUALITY

This specification describes display quality in case of no gray scale. Since display quality can be affected by gray scale methods, evaluate display quality forthe usability of the LCD unit in case gray scale is displayed on the LCD unit.

***WARNING***: Don't use any materials which emit gas from epoxy resin (Amines' hardener) and silicone adhesive agent (dealcohol or deoxym) to prevent polarizer color change caused by gas.

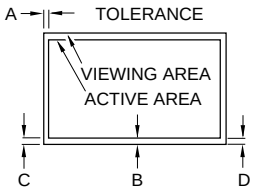
## OUTLINE DIMENSIONS




① CCFT CONNECTOR
PIN LAYOUT
(3 pins)

| PIN # | 1 | 2 | 3 |
|---|---|---|---|
| SYMBOL | HV | NC | GND |

② CCFT CABLE
UL3239, AWG22
(NISSEI ELECTRIC, LTD)




INTERFACE CONNECTOR
DF9D-31P-1 V (HIROSE)
PIN LAYOUT

| PIN # | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $DL_4$ | GND | $DL_5$ | YD | $DL_6$ | LP | $DL_7$ | GND | GND | XCK | $DL_0$ | $V_{CON}$ | $DL_1$ | $V_{DD}$ | GND |
| 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| $V_{DD}$ | DL2 | DISP | $DL_3$ | NC | GND | $DU_3$ | $DU_4$ | $DU_2$ | $DU_5$ | $DU_1$ | GND | $DU_0$ | $DU_6$ | GND | $DU_7$ |

**NOTES:**
1. Tolerance X-Direction A: 1.5 ±0.8
2. Tolerance Y-Direction B: 1.5 ±0.8
3. Obliquity of display area IC-DI <0.8
4. Unspecified Tolerance to be ±0.5

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